In the Claims

The following pending claims, claims 1-41, are presented for the Examiner's convenience:

1. A method for selecting components for a matched set comprising the steps of:

electrically and mechanically coupling a semiconductor wafer having a plurality of integrated circuit chips to an interposer to form a wafer-interposer assembly;

simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies; and

selecting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing.

2. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

3. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

4. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

5. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

6. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for performance over a range of temperatures.

7. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously performing burn-in testing of the at least two of the integrated circuit chips.

8. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously vibrating the at least two of the integrated circuit chips.

9. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for leakage currents.

10. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for offset voltages.

11. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for gain tracking.

12. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for bandwidth.

13. The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for speed grades.

14. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

15. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are analog devices.

16. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

17. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are mixed signal devices.

18. A method for assembling a matched set comprising the steps of:

providing a semiconductor wafer having a plurality of integrated circuit chips;

electrically and mechanically coupling the wafer to an interposer to form a wafer-interposer assembly;

simultaneously testing pairs of the integrated circuit chips of the wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies;

sorting the chip assemblies based upon the simultaneous testing of the pairs of the integrated circuit chips; and

electrically coupling at least two of the chip assemblies corresponding to a sorted pair of the integrated circuit chip onto a substrate, thereby assembling the matched set.

19. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

20. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of integrated

circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

21. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

22. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

23. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for performance over a range of temperatures.

24. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips

further comprises simultaneously performing burn-in testing of the pairs of the integrated circuit chips.

25. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously vibrating the pairs of the integrated circuit chips.

26. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for leakage currents.

27. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for offset voltages.

28. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for gain tracking.

29. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for bandwidth.

30. The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for speed grades.

31. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

32. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer analog devices.

33. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer mixed signal devices.

34. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

35. A matched set assembled by the method as recited in claim 18.

36. A matched set of integrated circuit chips comprising:

a first chip assembly diced from a wafer-interposer assembly, the first chip assembly including a first integrated circuit chip from a wafer;

a second chip assembly diced from the wafer-interposer assembly, the second chip assembly including a second integrated circuit chip from the wafer, the first and second integrated circuit chips being previously simultaneously tested as part of the wafer-interposer assembly; and

a substrate on to which the first and second chip assemblies are electrically coupled.

37. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

38. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are analog devices.

39. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

40. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are mixed signal devices.

41. The matched set as recited in claim 36 further comprising a third chip assembly diced from the wafer-interposer assembly, the third chip assembly including a third integrated circuit chip from the wafer, the first, second and third integrated circuit chips being previously simultaneously tested as part of the wafer-interposer assembly, the third chip assembly electrically coupled to the substrate.

Remarks

The Examiner has rejected claims 1-41 under 35 U.S.C. §102(e) as being anticipated by Razon et al., U.S. Patent No. 6,136,681, (hereinafter "Razon"). The Examiner has rejected claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Lam, U.S. Patent No. 6,281,046, (hereinafter "Lam") in view of Applicant's disclosure on pages 2-4 of the Specification.

Claims 1-41 were originally presented for Examination. Claims 1-41 are currently pending, of which, claims 1, 18, 35 and 36 are in independent form. Favorable reconsideration of the present amendment as currently constituted is respectfully requested.